International Journal of Thermophysics, Vol. 27, No. 1, January 2006 (© 2006)
DOI: 10.1007/s10765-006-0028-3

Heat Transfer in Fast Linear Annealing for Direct Bonding of SOI Wafer Pairs[1]

Youngcheol Joo[2,3] and Oh-Sung Song[4]

A novel silicon-on-insulator (SOI) manufacturing method, the fast linear annealing (FLA) method, is proposed. In the fast linear annealing method, a halogen lamp moves with a constant speed above a silicon wafer pair prebonded by the hydrogen interaction. In order to optimize the processing parameters such as the initial heat treatment time and the moving speed of the halogen lamp, bonding strengths were measured when the moving speed varies in the range of 0.05–0.5 $mm \cdot s^{-1}$. The temperature distribution of SOI is analyzed numerically by using a finite difference method. The SOI is modeled two-dimensionally, and the alternate direction implicit (ADI) technique is used for the calculation of the temperature. The calculation results show that the SOI reaches a steady-state temperature distribution in an elapsed time of 380 s of halogen lamp irradiation. The maximum temperature of SOI does not vary significantly as the moving speed of the halogen lamp increases. These results agree with the measurement results, which show that the bonding strength from the high-speed anneal (0.5 $mm \cdot s^{-1}$) was of similar strength to that from the slow speed (0.05 $mm \cdot s^{-1}$) process.

KEY WORDS: alternate direction implicit (ADI) method; direct bonding; fast linear annealing; finite difference method; silicon-on-insulator (SOI) wafer pairs.

[1] Paper presented at the Seventh Asian Thermophysical Properties Conference, August 23–28, 2004, Hefei and Huangshan, Anhui, P. R. China.

[2] Department of Mechanical Engineering, Soonchunhyang University, Shinchang-myun, Asan-si, Chungnam 336-745, Korea.
[3] To whom correspondence should be addressed. E-mail: ychjoo@sch.ac.kr
[4] Department of Materials Science and Engineering, University of Seoul, Cheonnong-dong, Tongdaemun-gu, Seoul 130-743, Korea.

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1. INTRODUCTION

Silicon-on-insulator (SOI) wafers are promising to enhance the speed of the devices up to 30% by reducing the wafer leakage current [1]. The direct bonding technology has overcome the practical problems of the previous SIMOX [2] and anodic bonding [3] of surface damages and dopants redistribution.

A micro-electro-mechanical system (MEMS) typically utilizes multilayer thin films consisting of $Si/SiO_2 \| Si_3N_4/Si$ in fabricating micro-cantilevers [4] or micro-pumps [5]. In order to expedite the fabrication, the direct bonding of different silicon surfaces at lower temperatures is of great interest [6].

The direct bonding of wafers was first introduced in 1985 and 1986 by two independent researchers: Shimbo [7] and Lasky [8]. Surfaces of two wafers are cleaned and physically brought together so that two wafers can be bonded together through van der Waal interactions or hydrogen bonding. The weakly bonded surfaces are subsequently thermally treated in order to increase the bonding strength. For Si wafers, temperatures in excess of 1100°C are typically required to provide sufficient interfacial strength [9]. Today the technology has been extended to other materials as well as heterogeneous surfaces [10].

Especially, since the invention of the smart-cut method [11] in which a Si thin film is split from the SOI substrate utilizing the ion implantation and hydrogen embrittlement effect to produce cheap and reliable SOI wafers, direct wafer bonding has become one of the key technologies in the semiconductor industry.

Conventional electric furnace annealing (CFA) is well known and a popular annealing method for oxidation and diffusion in semiconductor processing. It offers a batch process suitable for mass production and uniform heat distribution for all wafers. However, it takes a long time to ramp up and ramp down the heat and has to be maintained a relatively long time at high temperature, which may lead to a warpage problem.

Rapid thermal annealing (RTA) became popular in semiconductor processes recently. It offers quick annealing for each wafer within 30 s. However, almost no studies on direct bonding for the heterogeneous insulator SOI wafer pair with RTA is available.

Recently, we proposed a fast linear annealing (FLA) process that employs a single halogen lamp with a half-elliptic mirror to heat treat the directly bonded wafers as shown in Fig. 1. The combination provides a concentrated heat source that can be scanned over the substrate in order to generate rapid thermal annealing effects. Compared to conventional furnace annealing, the fast linear annealing method may be effective in removing the gaseous interface defects [12].

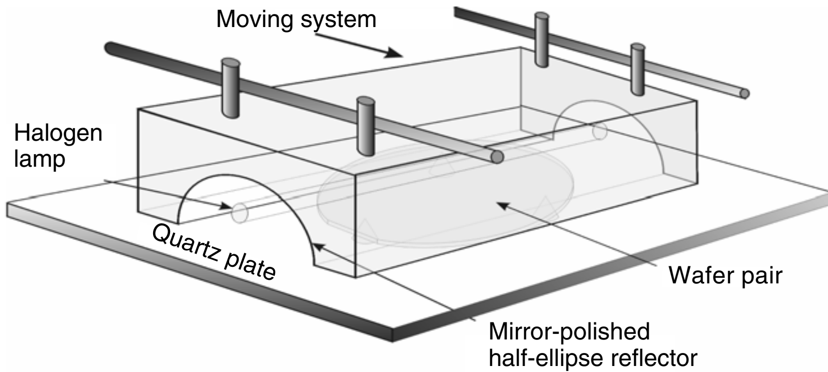


Fig. 1. Schematic diagram of fast linear annealing system.

The quartz stage of 300 mm diameter supports the premated substrate during scanning with three small quartz cones. The halogen lamps and mirror unit moves with a speed of 0.05–0.5 $mm \cdot s^{-1}$ by a motor. The stage and lamp units are water-cooled during the annealing. Once the substrate is located on the stage, the lamp is turned on to preheat and scan, then turned off to cool the substrate.

The aim of our work is to reduce the FLA process time by optimizing the preheating time and scan speed, and the major FLA process variables, through computer simulation with the input data based on FLA experiments.

2. EXPERIMENTAL PROCEDURES

2.1. SOI Manufacturing Method

About 2000 Å thick SiO_2 thermal oxide was grown on *p*-type Si(100) wafers with a diameter of 100 mm using dry O_2. The thickness of the thermal oxide was measured using an ellipsometer at 20 different locations for each wafer. Wafers whose thickness variation of the deposited films was less than 7% over the entire surface were used for the subsequent direct bonding experiment.

The SiO_2/Si wafers were cleaned with a mixture of H_2SO_4 and H_2O_2 in the ratio of 4:1 and deionized water. After the cleaning process, the wafers were dried in a spin dryer in order to activate the OH-surface species.

The cleaned wafer pair was immediately brought in contact in a Class #100 clean room using an aligner at room temperature. Using an IR camera as shown in Fig. 2, it was ensured that no air traps or voids

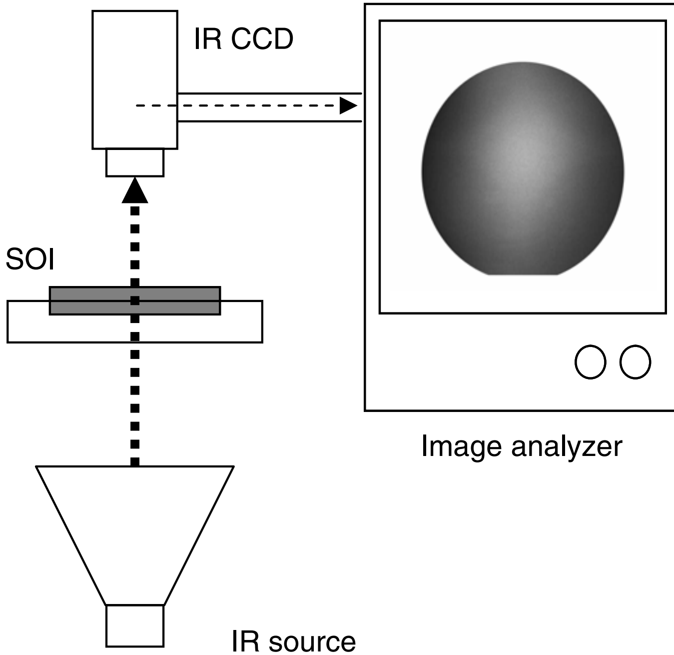


Fig. 2. Schematic diagram of IR image analyzer.

existed at the interface of the wafer pair prior to annealing. The wafer pairs with the bonded area exceeding 90% were used for the subsequent annealing process. The IR camera system was composed of an infrared source and an IR CCD camera. The transmitted IR beam through the SOI specimen was detected and visualized using a monitor with sharp contrast when voids existed.

The bonded wafers were annealed using the fast linear annealing (FLA) method. The lamp power was varied from 320 to 550 W, and the scan speed from 0.05 to 0.5 $mm \cdot s^{-1}$, respectively. The entire annealing process was finished in 125 s. Thermocouple sensors were located on the substrate bottom in every 5 mm scan direction to measure the real temperatures. They are used for the simulation input data. The bonded area was verified using an IR camera and image analyzing software, and the bonding strength was measured with the razor-blade crack-opening method [13].

2.2. Optimization of FLA Process Variables by Numerical Simulation

When a halogen lamp irradiates the silicon wafer, the temperature gradient of the silicon wafer in the halogen lamp axial direction is much

smaller than the temperature gradient in the halogen lamp movement direction. The SOI is modeled as two silicon wafers, whose thicknesses are 0.5 mm, lengths are 100 mm, and widths are infinity, which are in contact each other. The gap of the contact surface is assumed to be 5 Å and to be filled with water vapor.

The thermal radiation energy irradiated from the halogen lamp reaches the top surface of the silicon wafer directly or is reflected by an ellipsoidal reflection mirror. The radiation energy is a maximum at the focus of the ellipsoidal reflection mirror, and decreases gradually as the distance from the focus increases. The thermal radiation energy that is irradiated at the top surface of the silicon wafer directly and indirectly is assumed to have a distribution represented by a cosine function. The distribution of thermal radiation energy $q_r(x)$ is

$$\begin{aligned} q_r(x) &= \frac{1}{2} q_{r,\max} \times \left(\cos \frac{\pi (x - x_0)}{B} + 1 \right) && \text{for } x_0 - \frac{B}{2} \leqslant x \leqslant x_0 + \frac{B}{2} \\ &= 0 && \text{for } x < x_0 - \frac{B}{2},\ x > x_0 + \frac{B}{2} \end{aligned} \tag{1}$$

where

$q_{r,\max}$ is the peak radiation energy of the halogen lamp at the focus of a half elliptic reflector, which is directly under the halogen lamp;

x is the distance from the edge of the silicon wafer;

x_0 is the position of the focus of a half elliptic reflector; and

B is the bandwidth of the halogen lamp radiation energy.

The heat transferred from the top and bottom surfaces of SOI to the environment is by convective heat transfer and thermal radiation mechanisms. The heat transfer from the side of the silicon wafer to the environment is assumed to be negligibly small, because the surface area of the side is much smaller than that of the top and bottom.

When a horizontal plate is heated, the heat transfer from the upper surface can be obtained from the following equations [14, 15]:

$$\text{Laminar flow}: Nu = 0.54\,(Gr_L Pr)^{1/4} \quad 10^5 < Gr_L Pr < 2 \times 10^7 \tag{2}$$

$$\text{Turbulent flow}: Nu = 0.14\,(Gr_L Pr)^{1/4} \quad 2 \times 10^5 < Gr_L Pr < 3 \times 10^{10} \tag{3}$$

where Nu, Gr_L, and Pr are the Nusselt number, the Grashof number, and the Prandtl number, respectively. Because the $Gr_L Pr$ of FLA of the

present study is 7.9×10^5, the air flow on top of the SOI is laminar. Therefore, the convective heat transfer coefficient h can be expressed as

$$h = kNu/L = 8.713 \text{ W} \cdot \text{m}^{-2} \cdot \text{K}^{-1} \tag{4}$$

where k is the thermal conductivity of air and L is the length of the silicon wafer.

The convective heat transfer from the bottom surface of the heated horizontal plate can be obtained from the following equation:

$$\text{Laminar flow}: Nu = 0.27\,(Gr_{\text{L}}Pr)^{1/4} \quad 10^5 < Gr_{\text{L}}Pr < 2 \times 10^7 \tag{5}$$

The convective heat transfer coefficient for the bottom surface of SOI, $h = 4.357 \text{ W} \cdot \text{m}^{-2} \cdot \text{K}^{-1}$, is obtained from the above equation.

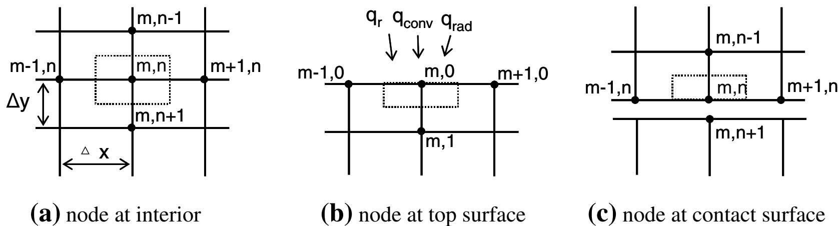
The energy balance method is used to obtain the finite difference equations of the numerical simulation of the temperature distribution of SOI. When we consider a control volume, a general form of the energy balance equation may be expressed as

$$\dot{E}_{\text{in}} = \dot{E}_{\text{st}} \tag{6}$$

where $\dot{E}_{\text{in}}$ is the energy transferred from the surroundings to the control volume, and $\dot{E}_{\text{st}}$ is the energy stored at the control volume [16, 17].

2.2.1. Nodes at Interior of Silicon Wafer

Assume a node *m, n* and a control volume that surrounds the node and has an area of $\Delta x \Delta y$ as shown in Fig. 3. When an energy balance equation is applied to the control volume,



(a) node at interior **(b)** node at top surface **(c)** node at contact surface

Fig. 3. Nodes and control volumes.

$$k\Delta y \frac{T_{m-1,n}^{p+1} - T_{m,n}^{p+1}}{\Delta x} + k\Delta y \frac{T_{m+1,n}^{p+1} - T_{m,n}^{p+1}}{\Delta x} + k\Delta x \frac{T_{m,n-1}^{p+1} - T_{m,n}^{p+1}}{\Delta y}$$
$$+ k\Delta x \frac{T_{m,n+1}^{p+1} - T_{m,n}^{p+1}}{\Delta y} = \rho C_p \Delta x \Delta y \frac{T_{m,n}^{p+1} - T_{m,n}^{p}}{\Delta t} \quad (7)$$

where ρ and C_p are the density and specific heat of the silicon wafer. The first term of the left-hand side of the equation signifies the energy transfer from the left side to the control volume, and the next terms signify the energy transfer from the right, top, and bottom to the control volume, respectively. The right-hand side of the equation signifies the energy stored in the control volume during the time step. T^p and T^{p+1} are the temperatures of node *m, n* at time *p* and that at one time step later.

2.2.2. Nodes at Top and Bottom Surfaces of SOI

Because a node $m, 0$ at the top surface of SOI is in contact with the surrounding air, the area of the control volume is $\Delta x \frac{\Delta y}{2}$. When the energy balance equation is applied to the control volume, we obtain the following equation:

$$k\frac{\Delta y}{2}\frac{T_{m-1,0}^{p+1} - T_{m,0}^{p+1}}{\Delta x} + k\frac{\Delta y}{2}\frac{T_{m+1,0}^{p+1} - T_{m,0}^{p+1}}{\Delta x} + k\Delta x \frac{T_{m,1}^{p+1} - T_{m,0}^{p+1}}{\Delta y}$$
$$+ h\Delta x \left(T_\infty - T_{m,0}^{p+1}\right) + \varepsilon\sigma\Delta x \left(T_\infty^4 - T_{m,0}^{4,p+1}\right) + q_r \Delta x$$
$$= \rho C_p \frac{\Delta x}{2} \Delta y \frac{T_{m,n}^{p+1} - T_{m,n}^{p}}{\Delta t} \quad (8)$$

The first three terms on the left-hand side of the equation signify the heat transfer from the left, right and bottom to the control volume of node $m, 0$, respectively. The next two terms represent the natural convection and radiation heat transfer from the environment. The last term signifies the irradiated energy of the halogen lamp. The term on the right-hand side of the equation signifies the energy stored in the control volume during the time step.

The finite difference equations for the nodes at the bottom surface of SOI are obtained with a similar method with Eq. (8).

2.2.3. Nodes at the Contact Surface

It is assumed that there is 5 Å thickness of water vapor at the contact surface between the upper and lower silicon wafers. The heat transfer at the contact surface per unit depth, q_{contact}, can be expressed as follows:

$$q_{\text{contact}} = \frac{\Delta x}{R_{t,c}} \left(T_{m,n+1} - T_{m,n} \right) = k_c \Delta x \frac{T_{m,n+1} - T_{m,n}}{\Delta y_c} \tag{9}$$

where Δx is the area of the contact surface and $R_{t,c}$ is the contact resistance. k_c is the thermal conductivity of the material in the contact surface, which is water vapor with a thermal conductivity of $0.0422\,\text{W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$. Δy_c is the gap distance of the contact surface, which is 5 Å. Therefore,

$$\frac{1}{R_{t,c}} = \frac{k_c}{\Delta y_c} = \frac{0.0422\text{W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}}{5 \times 10^{-10}\text{m}} = 84.4 \times 10^{6}\text{W} \cdot \text{m}^{-2} \cdot \text{K}^{-1} \tag{10}$$

When we substitute the above equation into the energy balance equation,

$$\begin{aligned} &k\frac{\Delta y}{2}\frac{T_{m-1,n}^{p+1} - T_{m,n}^{p+1}}{\Delta x} + k\frac{\Delta y}{2}\frac{T_{m+1,n}^{p+1} - T_{m,n}^{p+1}}{\Delta x} + k\Delta x\frac{T_{m,n-1}^{p+1} - T_{m,n}^{p+1}}{\Delta y} \\ &\quad + \frac{\Delta x}{R_{t,c}}\left(T_{m,n+1}^{p+1} - T_{m,n}^{p+1}\right) = \rho C_p \Delta x \frac{\Delta y}{2}\frac{T_{m,n}^{p+1} - T_{m,n}^{p}}{\Delta t} \end{aligned} \tag{11}$$

is obtained. The first three terms on the left-hand side represent the heat transfer from the left, right, and upper nodes to the control volume of node *m, n*, respectively. The next term is the heat transfer from the bottom silicon wafer through the contact surface. The equations of nodes at the top surface of the bottom wafer are obtained by a similar method as with Eq. (11).

Equations (7), (8), and (11) have the shape of a two-dimensional parabolic equation. Many numerical methods have been proposed to solve two-dimensional parabolic equation problems, but among them, the alternating direction implicit (ADI) method is the most frequently used because it is unconditionally stable [18]. For Eq. (7), a time step is divided by two, and for the first half-time step, the following finite difference equation is applied in the horizontal direction:

$$\begin{aligned} &k\frac{\Delta y}{\Delta x}\left(T_{m-1,n}^{p+\frac{1}{2}} - 2T_{m,n}^{p+\frac{1}{2}} + T_{m+1,n}^{p+\frac{1}{2}}\right) + k\frac{\Delta x}{\Delta y}\left(T_{m,n-1}^{p} - 2T_{m,n}^{p} + T_{m,n+1}^{p}\right) \\ &\quad = \rho C_p \Delta x \Delta y \frac{T_{m,n}^{p+\frac{1}{2}} - T_{m,n}^{p}}{\Delta t/2} \end{aligned} \tag{12}$$

Then, for the second half-time step, the following equation is applied in the vertical direction:

$$k\frac{\Delta y}{\Delta x}\left(T_{m-1,n}^{p+\frac{1}{2}} - 2T_{m,n}^{p+\frac{1}{2}} + T_{m+1,n}^{p+\frac{1}{2}}\right) + k\frac{\Delta x}{\Delta y}\left(T_{m,n-1}^{p+1} - 2T_{m,n}^{p+1} + T_{m,n+1}^{p+1}\right)$$
$$= \rho C_p \Delta x \Delta y \frac{T_{m,n}^{p+1} - T_{m,n}^{p+\frac{1}{2}}}{\Delta t/2} \quad (13)$$

Similar methods are applied to the Eqs. (8) and (11), and equations for the first half-time step in the horizontal direction and the equations for the second half-time step in the vertical direction are obtained. At first, $T^{p+\frac{1}{2}}$ of all nodes is obtained by applying the horizontal direction finite difference equations, then T^{p+1} of all nodes is obtained by applying the vertical direction finite difference equations.

The accuracy of the numerical analysis program is confirmed by comparing the exact solution of the temperature distribution of a two-dimensional infinite plate. One surface of the plate is insulated, and heat is transferred to the environment by convection at the other surface. The temperature distribution obtained by the ADI methods show a difference of less than 0.1% in comparison with the temperature distribution obtained by an analytical method.

3. RESULTS

3.1. Experimental Results

Figure 4 shows the crack length evolution of the diameter of 100 mm SOI with scan speed in the crack opening method to evaluate the bond strength. All SOIs were preheated for 380 s at 100 V, and then scanned at speeds from 0.05 to 0.5 $\mathrm{mm \cdot s^{-1}}$. All samples show a constant crack length, which means that they are not dependent on the scan speed.

As the crack length is inversely proportional to the bond strength, we have expected that the crack length might decrease with scan speed. However, they showed almost identical bond strengths. Therefore, we may conclude that the high scan speed may be employed to reduce annealing time without deterioration of the bond strength.

3.2. Thermal Radiation Energy Distribution of Halogen Lamp

The temperature distribution of a silicon wafer is measured. The thermocouples are installed on the top surface of the silicon wafer at 5 mm distance increments in the halogen lamp movement direction. Figure 5

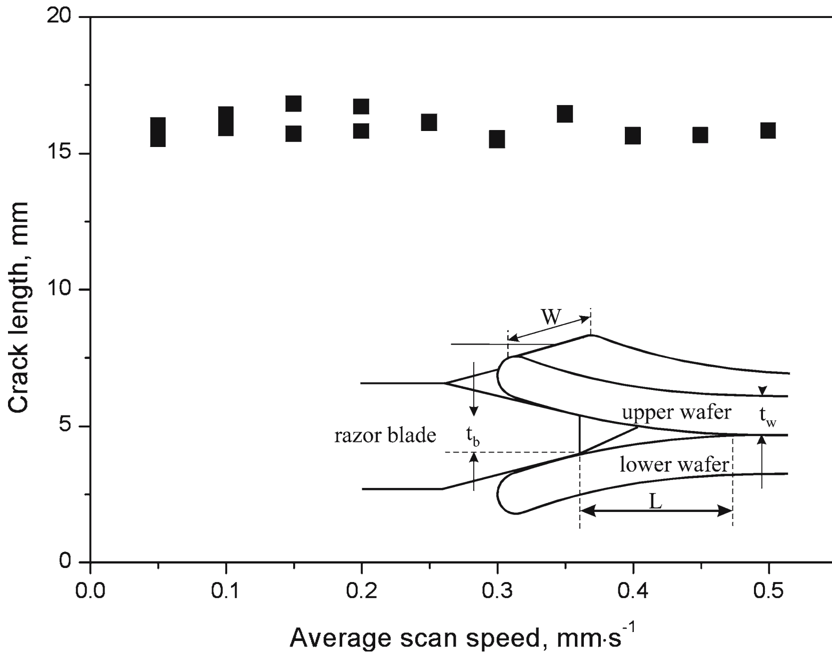


Fig. 4. Crack length distribution at different scan speeds of halogen lamp on the wafer created by razor-blade crack-opening method. Inset is the illustration of the crack opening method, which shows the crack length (L).

shows the measured temperature distribution when the halogen lamp is located at the center of the silicon wafer, and the input voltage is varied from 80 to 150 V. The x-coordinate indicates the distance from the elliptical reflector's focal point, and the y-coordinate is the measured temperature. The temperature of the silicon wafer increases as the halogen lamp input voltage increases. The temperature is a maximum at the focal point of the reflector, and decreases rapidly as the distance from the focal point increases and decreases gradually from a distance of about 20 mm.

Because the thermal radiation energy distribution irradiated from the halogen lamp and the elliptical reflector is difficult to measure directly, it is estimated by comparing the measured temperature distribution and the calculated values. The calculated temperature distribution is obtained by an FDM program on varying the peak value and the bandwidth of the thermal irradiated energy of a halogen lamp. The best fitted calculated temperature distribution with the measured data is found by trial and error. When the bandwidth is 12.5 mm and the peak values are 80 and $110\,\mathrm{kW \cdot m^{-2}}$, the calculated temperature distributions are consistent with

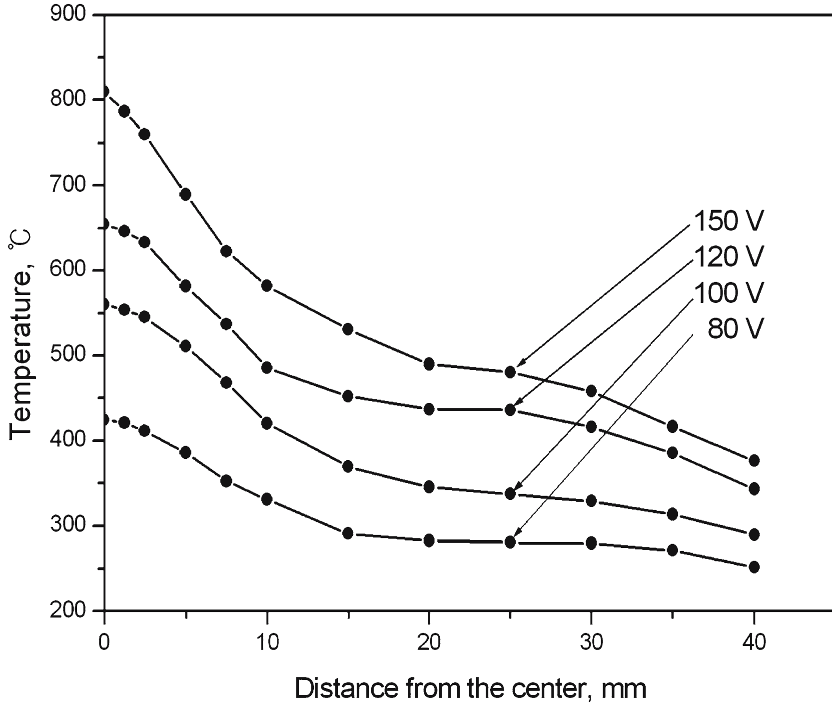


Fig. 5. Measured temperature distribution of silicon wafer.

measured values of 80 and 120 V. The bandwidth of 12.5 mm is used for further calculations of the temperature distribution.

3.3. Temperature Distribution of SOI at Initial Steady State

In a fast linear annealing method, the halogen lamp stays at one end of the silicon wafer for a certain period of time to reach the wafer temperature steady state. Then the lamp moves to the other end of the wafer at a constant speed. In order to simulate the initial steady state, the temperature distribution of SOI is calculated when the halogen lamp stays at a point 10 mm from the left end of the wafer.

Figure 6 shows the radiation energy distribution and the steady-state temperature distribution of the SOI contact surface when the halogen lamp stays at 10 mm distance from the left end of SOI. Because the distribution of the halogen lamp radiation energy is assumed to have a shape of a cosine function, the energy at the outside of the irradiation bandwidth of 12.5 mm is zero. The temperature at the area where the halogen lamp

radiation energy is irradiated is the highest, and it decreases as the distance from the halogen lamp increases. However, the point that shows a maximum temperature is not a point directly under the halogen lamp, but shifted a little to the left side. The reason is believed to be that the heat is accumulated at the left side because the convective and radiation heat transfer from the vertical surface of the edge to the environment is almost negligible compared to the conduction to the silicon wafer that occurred at the right side.

Figure 7a shows the vertical temperature distribution at a point under the halogen lamp, which is 10 mm from the left end of SOI. The temperature is the highest at the top surface of SOI, where the halogen lamp radiation energy is irradiated, and then decreases as the distance from the top surface increases. The temperature difference between the bottom surface of the upper wafer and the top surface of the lower wafer is only 0.0004°C. The temperature gradient near the bottom surface of SOI is smaller than that of the top surface, which indicates that the heat released from the bottom surface is smaller than the heat absorbed through the top

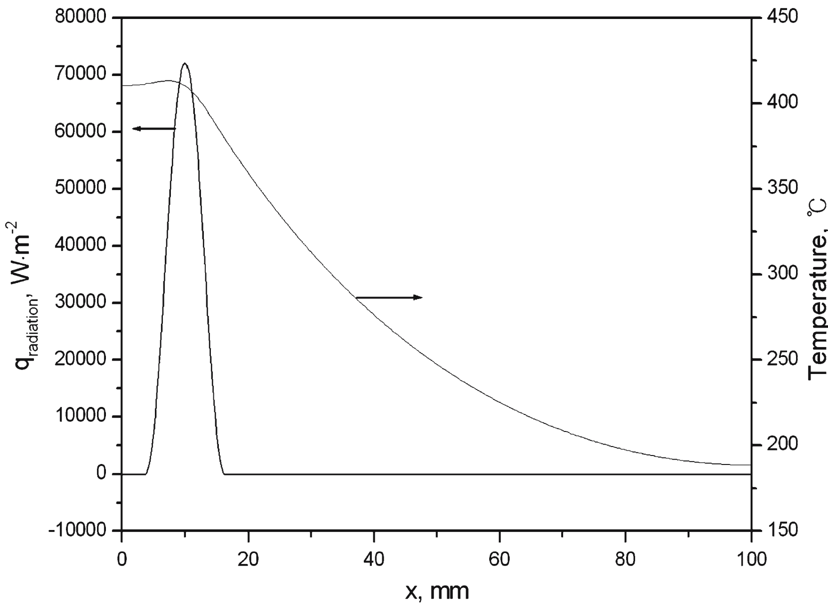


Fig. 6. Radiation energy distribution and steady-state temperature distribution of SOI when the halogen lamp stays at 10 mm distance from the left end of SOI.

surface. The remaining heat is transferred to the right and left sides of SOI by conduction.

Figure 7b shows the vertical temperature distribution of SOI at a point of $x = 90$ mm, far from the halogen lamp ($x = 10$ mm). The temperature inside the wafer is the highest, and it decreases to the top and bottom surfaces. This is because the radiation energy absorbed through the top surface area under the halogen lamp is transferred to the right side of SOI, and is released to the environment through the top and bottom surfaces of SOI. The reason that the temperature gradient at the upper wafer is larger than that at the lower wafer is that the heat loss at the top surface is larger than that at the bottom surface.

The time period to reach the SOI temperature steady state is investigated. The initial temperature of SOI was 23°C. After 300 s elapsed time of the halogen lamp irradiation, the temperature of the whole SOI is within 5°C from the steady-state temperature distribution. After 380 s, the whole region of SOI reaches within 2°C from the steady state. About 380 s can be assumed to be the elapsed time to reach a steady state from an engineering point of view. Thus, we selected an optimum preheating time of 380 s.

3.4. Temperature Distribution of SOI When the Halogen Lamp Moves at a Constant Speed

The temperature distribution of SOI is calculated when the halogen lamp moves to the right side at a constant speed. Figure 8a shows the variation of the contact surface temperature distribution at a halogen lamp speed of $0.05\,\mathrm{mm \cdot s^{-1}}$, which is the lowest speed of the present FLA system. Because the halogen lamp speed is very slow, the temperature distribution at each moment is similar to that of the steady state. When the halogen lamp is located at the center of the wafer, which is for $t = 800$ s, the temperature distribution of the contact surface is almost symmetrical. The maximum temperature at this time is lower than that when the halogen lamp is located near the left end of the wafer, because the heat irradiated from the halogen lamp at the middle section of SOI is transferred effectively to the left and right sides of SOI. When the halogen lamp is located at 90 mm, which is for $t = 1600$ s, the temperature distribution is almost symmetrical with that of the initial time.

Figure 8b shows the variation of the temperature distribution at a halogen lamp speed of $0.5\,\mathrm{mm \cdot s^{-1}}$, which is the maximum speed of the present FLA system. Because the halogen lamp speed is high, the asymmetry of the temperature distribution is increased. When the halogen lamp is located at the center of the wafer, which is for $t = 80$ s, the right-side

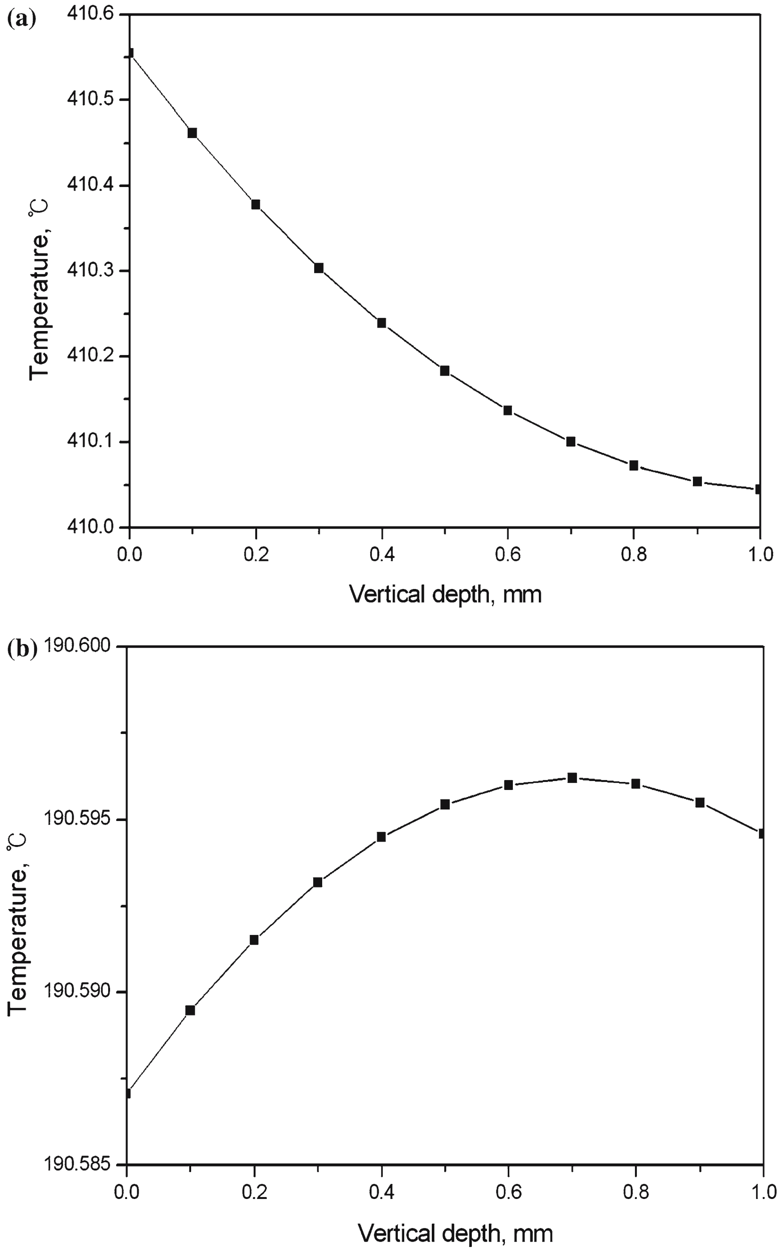


Fig. 7. Vertical temperature distribution of SOI (a) at a point under the halogen lamp ($x = 10$ mm) and (b) at a point far from the halogen lamp ($x = 90$ mm).

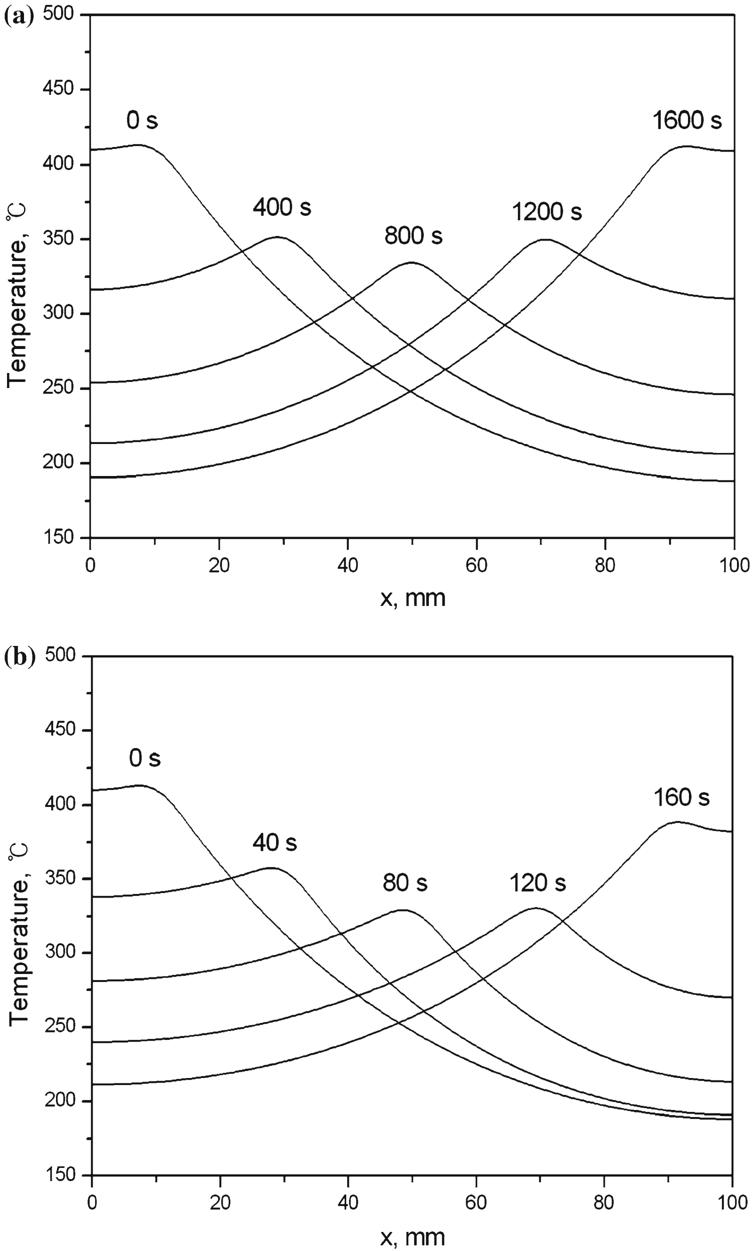


Fig. 8. Temperature distribution of SOI when the halogen lamp moves at a speed of (a) $0.05\,\mathrm{mm \cdot s^{-1}}$ and (b) $0.5\,\mathrm{mm \cdot s^{-1}}$.

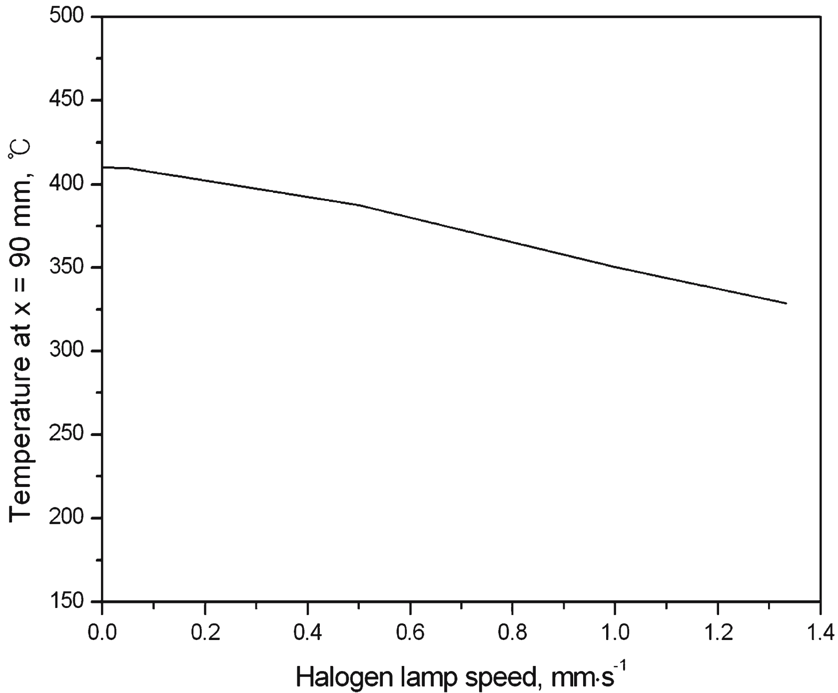


Fig. 9. Temperature of the silicon wafer with different moving speeds of the halogen lamp.

temperature gradient is larger than that of the left side. It is because the temperature at the right side is rising as the halogen lamp approaches, but the heat at the left side does not cool sufficiently as the halogen lamp moves away. When the halogen lamp reaches the right end of SOI, the maximum temperature is lower than that of the steady state. However, considering the halogen lamp speed is increased by a factor of 10, the decrease of the maximum temperature at the point of $x = 90\,\text{mm}$ is only 23°C.

Figure 9 shows the temperature of contact surface at the point of $x = 90\,\text{mm}$ when the halogen lamp is located above that point. The halogen lamp speed is varied from 0 to $1.33\,\text{mm} \cdot \text{s}^{-1}$. The temperature of the contact surface decreases as the halogen lamp speed increases, but the decrease is relatively small compared to the increase of the halogen lamp speed.

From the simulation results, it can be predicted that the increase of the halogen lamp speed does not affect the maximum temperature of the local contact surface because the thermal conductivity of the silicon wafer

is sufficiently large. It is believed that the halogen lamp speed is more related to the total heat input rather than the local maximum temperature, and the total maximum heat input affects the SOI annealing process.

4. CONCLUSION

A FDM computer program is developed to analyze the temperature distribution of SOI. The program is applied for the SOI manufacturing process by a fast linear annealing method. The time period required to reach the temperature of SOI steady state is calculated to be 380 s. When the halogen lamp velocity is increased, the SOI temperature is decreased, but the difference is small. The experimental results also support that the increase of the halogen lamp speed does not decrease the contact strength. Therefore, SOI can be manufactured without the loss of contact strength at a velocity of $0.5\,\mathrm{mm}\cdot\mathrm{s}^{-1}$, which is the maximum allowable speed of the present system.

ACKNOWLEDGMENTS

This work was supported by the grant No. R-12-2002-052-04003-0 from the Regional Research Center of the Korean Ministry of Commerce, Industry and Energy.

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